IN THE UN[illegible]D STATES PATENT AND TRAD[illegible]ARK OFFICE

Sub. 7
A4

09584424.101200

Please add the following new claims.

---

50. (New) The method of claim 49, wherein:

forming the multilayer gate dielectric includes forming a bottom dielectric, the charge storage layer over the bottom dielectric, and a top dielectric over the charge storage layer.

51. (New) The method of claim 50, wherein:

forming the bottom dielectric includes forming a layer of silicon dioxide.

52. (New) The method of claim 50, wherein:

forming the bottom dielectric includes thermally growing a layer of silicon dioxide.

53. (New) The method of claim 50, wherein:

forming the charge storage layer includes forming a layer selected from the group consisting of silicon nitride, silicon oxynitride, silicon-rich silicon dioxide, and a ferroelectric material.

54. (New) The method of claim 50, wherein:

forming the top dielectric includes forming a layer of silicon dioxide.

55. (New) The method of claim 54, wherein:

forming the top dielectric includes thermally growing a layer of silicon dioxide.

56. (New) The method of claim 54, wherein:

forming the top dielectric includes depositing a layer of silicon dioxide.

57. (New) The method of claim 49, wherein:

forming the gate includes forming a polycrystalline silicon gate doped to an n-type conductivity; and

the source and drain regions have a p-type conductivity.

58. (New) The method of claim 49, wherein:

forming the gate includes forming a polycrystalline silicon gate doped to a p-type conductivity; and

the source and drain regions have an n-type conductivity.

59. (New) The method of claim 49, wherein:

forming the gate includes forming a polycrystalline silicon gate having a dopant concentration greater than about 10^{10} atoms/cm^3.

~~60. (New) A method, comprising the steps of:~~

~~applying an electric field to a charge storage layer in a multilayer dielectric disposed between a first semiconductor layer and a second semiconductor layer to form a charge accumulation region in the first semiconductor layer proximate to the multilayer gate dielectric and a charge depletion region in the second semiconductor layer proximate to the multilayer gate dielectric.~~

~~61. (New) The method of claim 60, wherein:~~

~~the first semiconductor layer comprises a transistor gate; and~~

~~the second semiconductor layer comprises a transistor channel between a source and drain region.~~

~~62. (New) The method of claim 60, wherein:~~

~~the first semiconductor layer comprises a transistor channel between a source and drain region; and~~

~~the second semiconductor layer comprises a transistor gate.~~

~~63. (New) The method of claim 60, wherein:~~

~~the first semiconductor layer and second semiconductor layer are doped to a first conductivity type.~~

~~64. (New) The method of claim 60, wherein:~~

~~the applying step is conducted for a length of time sufficient to accumulate charge in a charge storage layer of the multilayer dielectric.~~

65. (New) The method of claim 64, wherein:

the applying step is conducted under conditions sufficient to tunnel electrons through a tunnel dielectric of the multilayer dielectric to the charge storage layer.

66 ~~65~~. (New) The method of claim 64, wherein:

the charge storage layer comprises silicon nitride.

67 ~~66~~. (New) The method of claim 60, wherein:

the first semiconductor layer comprises a p-type gate; and

the second semiconductor layer comprises a p-type channel disposed between n-type source/drain regions.

68 ~~67~~. (New) The method of claim 60, wherein:

the first semiconductor layer comprises an n-type gate; and

the second semiconductor layer comprises an n-type channel disposed between p-type source/drain regions.

69 ~~68~~. (New) The method of claim 60, wherein:

the multilayer gate dielectric comprises a charge storage layer selected from the group consisting of silicon nitride, silicon oxynitride, silicon-rich silicon dioxide, and a ferroelectric material.

A4

Rule 126

Sub